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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,029	12/22/2000	Ariel Cohen	00-177	4217

24319 7590 11/19/2003

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EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,029	COHEN ET AL.	
	Examin r	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2000 and 09 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Change of Address as received on 8/9/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The use of the trademark "picoJava" has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner that might adversely affect their validity as trademarks.

Claim Objections

6. Claims 11 and 16 are objected to because of the following informalities:

   a. Claim 11 recites the limitation "extension stack can be emptied/filled to/from a memory device." It is unclear whether this claim language comprises "emptied to", "emptied from", "filled to", and "filled from", as two of those four possibilities (emptied from and filled to) are counterintuitive to the common usage of the terms in the art. Please correct the claim language to more clearly state the operation that is being performed in claim 11.

   b. Claim 16 recites the limitation "stack management unit controls pushes/pops to/from said internal registers." It is unclear whether this claim language comprises "pushes to", "pushes from", "pops to", and "pops from", as two of those four possibilities (pushes to and pops from) are counterintuitive to the common usage of the terms "push" and "pop" in the art. Please correct the claim language to more clearly state the operation that is being performed in claim 16.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. The claim recites the limitation "means for manipulating data in response to instruction codes of a first instruction set comprising a number of internal registers." It is unclear as to whether the "number of internal registers" are comprised in an instruction set or not, as it is well known in the art that registers are comprised in the apparatus that executes an instruction set. For the purposes of the examination, the examiner will assume that the "number of internal registers" are included in the apparatus. Please correct the claim language to more clearly point out the claimed invention.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-12 and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al, U.S. Patent No. 6,332,215.

12. Regarding claim 1, Patel has taught an apparatus comprising:

a. A processor (26 of Fig.1):

i. Comprising a number of internal registers (see Col.4 lines 6-27 and 35-40).

ii. Configured to manipulate contents of said registers in response to instruction codes of a first instruction set (see Col.4 lines 9-12, 49-54).

b. A translator circuit configured to implement a stack using one or more of the internal registers of said processor (see Col.2 lines 6-13, 22-24, Col.3 lines 35-37 and Col.4 lines 1-4).

13. Regarding claim 2, Patel has taught the apparatus according to claim 1, wherein said registers are used to store a top of stack (see Col.4 lines 12-15).

14. Regarding claim 3, Patel has taught the apparatus according to claim 2, wherein said top of stack is a Java Virtual Machine (JVM) top of stack (see Col.4 lines 9-15).

15. Regarding claim 4, Patel has taught the apparatus according to claim 1, wherein said internal registers are dynamically allocated in response to stack status (see Col.5 lines 51-67 and Col.6 lines 1-11). Here it is shown that registers are allocated to contain new values as stack operations are performed and the need for the stack to "grow" is required.

16. Regarding claim 5, Patel has taught the apparatus according to claim 1, wherein said translator circuit generates one or more instruction codes of the first instruction set for controlling the internal registers in response to an instruction code of a second instruction set (see Col.4 lines 1-4, 49-54). Because the bytecode (second instruction set) is translated into native instructions (first instruction set) in order to be executed, and that the JVM hardware registers are updated after each bytecode is executed, it is inherent that the native instructions can access and control both the JVM registers (44 of Fig.3) and the Java CPU registers (48 of Fig.3).

17. Regarding claim 6, Patel has taught the apparatus according to claim 5, wherein said instruction code of said second instruction set is a stack instruction (see Col.4 lines 49-54). While not taught explicitly, it is inherent that instructions that operate on a stack can be considered "stack instructions."

18. Regarding claim 7, Patel has taught the apparatus according to claim 1, wherein said translator circuit comprises an extension stack (50 of Fig.3).

19. Regarding claim 8, Patel has taught the apparatus according to claim 7, wherein said translator circuit is configured to transfer values between said internal registers and said extension stack (see Col.4 lines 19-22). Because the internal registers are contained in the Java Stack (50 of Fig.3), and that the pointer to the top of the stack is held within the internal registers, it is inherent in the updating of the top of stack pointer that data will be transferred between locations in the stack and the top of the stack pointer register.

20. Regarding claim 9, Patel has taught the apparatus according to claim 7, wherein said extension stack (50 of Fig.3) is implemented as a last-in first-out (LIFO) memory. While it is not taught explicitly, it is inherent and is well known in the art that stacks are implemented as last-in first-out data structures.

21. Regarding claim 10, Patel has taught the apparatus according to claim 9, wherein said extension stack has both head (see "Optop" on Col.4 lines 14-15) and tail interfaces (see "Frame" on Col.4 lines 15-16).

22. Regarding claim 11, Patel has taught the apparatus according to claim 7, wherein said extension stack can be emptied/filled to/from a memory device (see Col.4 lines 19-22 and 54-57).

23. Regarding claim 12, Patel has taught the apparatus according to claim 11, wherein said memory device comprises a main memory of said processor (see Col.4 lines 54-57).

24. Regarding claim 14, Patel has taught the apparatus according to claim 1, wherein said translator circuit (42 of Fig.4) comprises a stack management unit (74 of Fig.4) configured to track which internal registers are used for the stack (see Col.5 lines 43-46).

25. Regarding claim 15, Patel has taught the apparatus according to claim 14, wherein said stack management unit (74 of Fig.4) is further configured to track how many internal registers are used for the stack (see Col.5 lines 34-37).

26. Regarding claim 16, Patel has taught the apparatus according to claim 14 as shown above, wherein said stack management unit (74 of Fig.4) controls pushes/pops to/from said internal registers (see Col.5 lines 43-46). While not taught explicitly, it is well known in the art that a stack has the ability to push and pop data between registers and the stack. Because the internal registers are contained in the Java Stack (50 of Fig.3), it is inherent that the push and pop operations will transfer data between the internal registers and the stack.

27. Regarding claim 17, Patel has taught an apparatus comprising:

a. Means for manipulating data in response to instruction codes of a first instruction set comprising a number of internal registers (see Col.4 lines 9-12, 49-54).

b. Means for using one or more of said internal registers as a top of stack (see Col.4 lines 12-15).

28. Regarding claim 18, Patel has taught a method for implementing a Java Virtual Machine top of stack comprising the steps of:

a. Translating one or more instruction codes of a first instruction set into sequences of instruction codes of a second instruction set (Col.3 lines 35-37 and Col.4 lines 1-4).

b. Manipulating contents of one or more internal registers of a processor in response to said sequence of instruction codes of said second instruction set (see Col.4 lines 9-12, 49-54).

29. Regarding claim 19, Patel has taught the method according to claim 18, wherein said instruction codes of said first instruction set comprise stack operations. It is well known in the art that instructions that are executed on the Java Virtual Machine as in claim 18 are stack-based. That is, their operands are found on the stack rather than in registers. It is therefore inherent that any non-trivial instructions of the Java instruction set (first instruction set) will be "stack operations" due to their stack-based nature.

30. Regarding claim 20, Patel has taught the method according to claim 18, further comprising the step of:

a. Transferring contents of said internal registers to an extension stack or a memory device in response to said sequence of instruction codes of said second instruction set (see Col.4 lines 19-22 and 54-57).

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al, U.S. Patent No. 6,332,215, in further view of Tremblay et al, U.S. Patent No. 6,021,469.

33. Regarding claim 13, Patel has taught the apparatus according to claim 7 as shown above, wherein said extension stack is configured to indicate an empty or full condition. Patel has not taught the extension stack indicating an almost empty or almost full condition.

34. However, Tremblay has taught the use of high and low watermarks to indicate when the stack is near full or empty so to avoid overflows or overwrites (see Col.18 lines 46-51). Therefore, it would have been obvious to modify Patel to include high and low watermarks as Tremblay does to more clearly indicate when a potential overflow or overwrite condition occurs.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

36. Lindwer, U.S. Patent No. 6,298,434, has taught the processing of virtual machine instructions in a dedicated processor after converting virtual machine instructions into native language instructions.

37. Poff et al, U.S. Patent No. 6,330,659, has taught a method for accelerating the execution of java-like instructions in hardware.

38. Gee et al, U.S. Patent No. 6,374,286, has taught a processor capable of running multiple java virtual machines in hardware concurrently.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
11/10/2003

EDDIE CHAN
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